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## Parameter comparison for low-noise Mo/Au TES bolometers

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### Abstract

We describe a comparative investigation of the parameters of MoAu-bilayer TES bolometers designed for infrared detectors. A set of devices with variations in geometry were fabricated at the NASA/GSFC detector development facility. These detectors have different bilayer aspect ratios (providing differing normal state resistances and current densities), and have varieties of normal metal regions to study the effects of geometry on noise. These normal metal regions are oriented either parallel to or transverse to the direction of current flow, or both. The lowest noise detectors are found to have normal metal regions oriented transversely. For about a dozen different devices, we have measured a large set of parameters by means of a suite of tests. These include complex impedance measurements to derive time constants; *IV* curves to determine resistance and power; thermal conductance measurements; noise measurements as a function of device resistance; and direct resistance vs. temperature measurements.

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### 1. Introduction

The development of large format (>100 element) cryogenic bolometer arrays is a requirement for future astronomical imaging and spectroscopy in the far-infrared and submillimeter. Recent research has led to a new approach to building arrays of many bolometers. Instead of a semi-conducting thermistor, a superconducting transi-

tion edge sensor (TES) is used to read out the detector temperature. A TES bolometer has a faster response time than an identically designed, same-sensitivity semiconducting bolometer (or a more sensitive bolometer for the same response time) due to the strong negative electrothermal feedback intrinsic in a voltage-biased TES [1]. TES bolometers are inherently low impedance devices, so they are well-matched to being read out by DC SQUID amplifiers [2]. These amplifiers have a large noise margin over the TES Johnson noise and bolometer phonon noise. This permits the bolometer to be read out in a multiplexed fashion

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by a suitable SQUID multiplexer [3], potentially vastly reducing the amplifier size and the wire count. In light of these advantages, we have been developing the technologies for fabricating multiplexed superconducting TES bolometer arrays. Herein, we describe recent progress on the TES bolometers we have manufactured and tested.

Attempts to find robust materials systems and fabrication methods for TES bolometers have often resulted in detectors with excess noise or other, often milder, pathologies. This has been the case for devices manufactured using different materials, designs and fabrication approaches, including those made at NASA/GSFC and elsewhere [4,5]. We have recently made an effort to quantify, in a limited set of designs, the effect of various design geometries on the excess noise. Our simplest molybdenum and gold superconducting bilayers exhibit a large (as much as 10x) excess noise component. We have shown that certain geometries of normal metal boundary conditions imposed on the bilayer can reduce the excess noise problems. This result may be relevant to other materials systems and detector geometries.

## 2. Bolometer design

The bolometers are based on a linear  $1 \times 8$  design, using a pop-up-detector architecture first presented elsewhere [6] (Fig. 1). On each pixel is a different TES bilayer; two different  $1 \times 8$  arrays

were manufactured. A subset of the resultant 16 geometries is shown below in Fig. 2. A description of the fabrication process is given elsewhere [7].

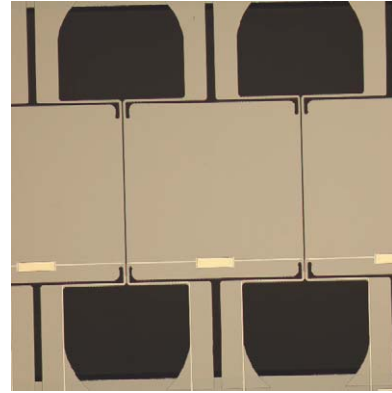


Fig. 1. Photo of single bolometer in a linear  $1 \times 8$  array.

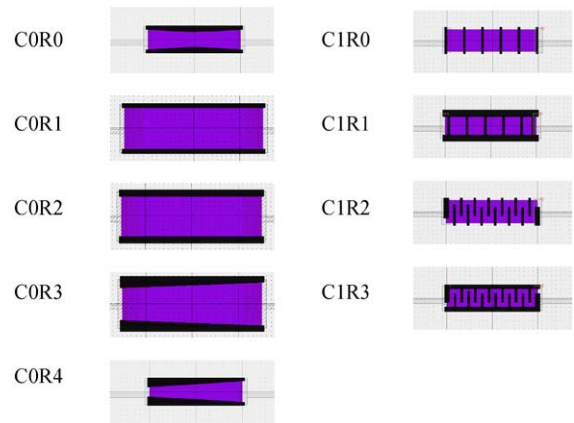


Fig. 2. Devices tested to date, showing (L) lateral bars and (R) interdigitated transverse bars.

Table 1  
Summary of measurements on TES bolometers

Geometry	$R_N$ (m $\Omega$ )	$T_C$ (mK)	$\alpha$	$G(T_C)$ [W/K]	Bias power (pW)	$\tau_e$ (ms)	Excess noise <sup>a</sup>
C0R0	539	504.5	5506	$0.84 \times 10^{-9}$	61	0.18	$\sim 3.5 \times$
C0R1	419	505.8	2771	$1.10 \times 10^{-9}$	65	0.17	$\sim 2.5 \times$
C0R2	500	506.0	6787	$0.87 \times 10^{-9}$	63	0.24	$\sim 2.5 \times$
C0R3	422	$\sim 490$	—	$1.12 \times 10^{-9}$	52	0.24	$\sim 2.5 \times$
C0R4	554	$\sim 490$	—	$0.92 \times 10^{-9}$	60	0.17	$\sim 7.5 \times$
C1R0	361	—	—	—	31	—	—
C1R1	212	436.1	89	—	30	—	—
C1R2	420	445.0	148	$0.44 \times 10^{-9}$	37	0.16	$< 50\%$
C1R3	401	$\sim 435$	—	$0.38 \times 10^{-9}$	35	0.10	$\leq 10\%$

<sup>a</sup> Excess noise is estimated maximum noise level relative to the theoretical prediction, at any frequency in the range 100 Hz–25kHz.

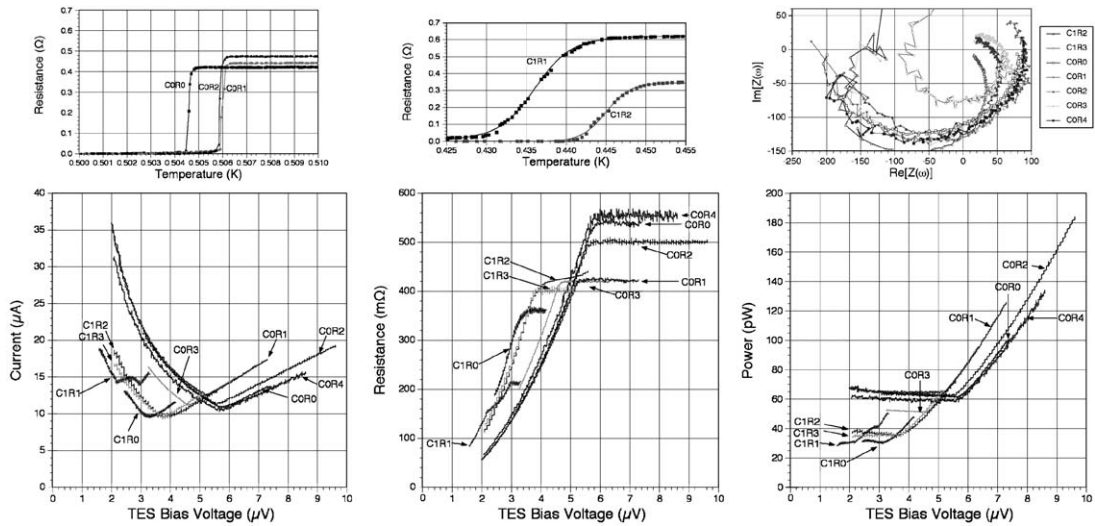


Fig. 3. Measurements of devices, illustrating parameter variations.

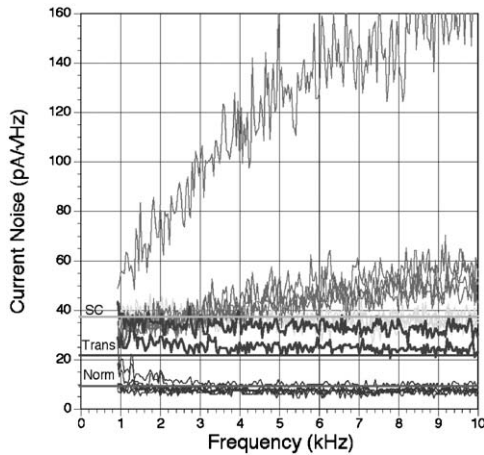


Fig. 4. Noise measurements of devices, illustrating superior performance for C1 (transverse bar) devices (heavy grey lines) as compared to C0 (lateral bar) devices (light grey lines).

### 3. Device characterization

Several standard measurements are used to characterize the devices. These include: (1) four-wire resistance vs. temperature measurements, with variable current excitation; (2) current–voltage ( $IV$ ) curves, with variable base temperatures; (3) noise measurements, with variable bias conditions; (4) complex impedance measurements, with variable bias conditions, as

described by Lindeman et al. [8]. Some representative results of these measurements are tabulated in Table 1. Stagnun et al. [9] present a more comprehensive discussion of the noise measurements. We show below a sample of  $R(T)$ ,  $R$  vs.  $V$ ,  $P$  vs.  $V$ ,  $G(T)$ , noise measurements, and  $Z(\omega)$  measurements (Fig. 3).

Devices from chip C0 tend to have more uniformity of parameters, and sharper  $R(T)$  transitions. Devices labeled C1 tend to have less noise (Fig. 4).

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